CLAIMS

1. Process for the sequential addressing of the inputs of a multiplexer (2) which comprises several stages (30, 31, 32) of switches from its inputs to its output and which is addressed at the level of each stage of switches by an elementary counter (11, 12 or 13) provided with a counting input, with a reinitialization input, with counting outputs controlling the switches of the relevant stage (30, 31, 32) and with an overflow output, and chained to the elementary counters of the lower stages of switches by linking its counting input to the overflow output of the elementary counter of the lower stage so as to constitute a global addressing counter, the said process being characterized in that it consists:

- in using, for the addressing of the stage (30) of switches of lower level closest to the inputs of the multiplexer (2), an elementary counter (11, 14) having a capacity or counting cycle length which can be adjusted on command,
- in providing controllable circuits (15) for shunting the elementary counters (12) of the stages (31) of intermediate switches,
- in periodically generating a counting order for the counting input of the elementary counter (11) of the stage of switches of lower level so as to make it describe successive counting cycles,
- in altering the configuration of the global addressing counter, at the start of each of the counting cycles of the elementary counter (11) of the stage of switches of lower level, by acting on the length of the forthcoming counting cycle of this elementary counter (11, 14) of the stage of switches of lower level as well as on the in-activity shunting circuits (15) of the elementary counters of the stages of intermediate switches.

2. Process according to claim 1, characterized in that the successive reconfigurings of the global

counter (11, 12, 13) for addressing the multiplexer (2) occurring in the course of a scanning sequence for the inputs of the multiplexer, are defined with the aid of a string of instructions written in a binary reconfiguring language comprising code words for adjusting the length of the counting cycle of the elementary counter (11, 14) catering for the addressing of the stage (30) of switches of lower level and code words for activating or inhibiting the controllable shunting circuits (15) of the elementary counters (12) catering for the addressing of the stages (31) of intermediate switches.

3. Process according to claim 2, characterized in that the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) also comprises code words for activating or inhibiting a mode for repeating or for retaining the length of the counting cycle of the elementary counter (11, 14) catering for the addressing of the stage (30) of switches of lower level and a repetition code word valid only when the repetition mode is active.

4. Process according to claim 2, characterized in that the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) comprises an end code word indicating the end of a string of configuration instructions.

5. Process according to claim 2, characterized in that the various code words of the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) are binary code words of variable lengths, the code words most frequently used having the shortest lengths.

6. Process according to claim 3, characterized in that the various binary code words of the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) all begin with a 0 with the exception of the code word for inhibiting a repetition mode.

7. Process according to claim 3, characterized in that the repetition code word in the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) is logical 0.

8. Process according to claim 3, characterized in that the code word for inhibiting the repetition mode in the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) is logical 1.

9. Process according to claim 3, characterized in that the code word for activating the repetition mode in the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) is binary 01.

10. Process according to claim 3, applied to a multiplexer (2) with three stages (30, 31, 32) of switches, characterized in that the code words for activating and for inhibiting the controllable circuit (15) for shunting the elementary counter (12) addressing the second stage (31) of switches in the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) coincide and are expressed by the binary word with four bits 0001, this binary word signifying a change of the active or inactive state of the shunting circuit (15) of the elementary counter (12) addressing the second stage (31) of switches.

11. Process according to claim 4, characterized in that the end code word in the language for reconfiguring the global counter (11, 12, 13) for addressing the multiplexer (2) is a string of binary zeroes.

12. Addressing device for a multiplexer (2) having a staged architecture with several stages (30, 31, 32) of switches from its input to its output, comprising a global counter (10) consisting of a chaining of elementary counters (11, 12, 13) each addressing a stage (30, 31, 32) of switches of the multiplexer (2), characterized in that it comprises a

global counter (10) with an elementary counter (11) having counting capacity which can be adjusted on command for the addressing of the stage (30) of switches of lower level closest to the inputs of the multiplexer (2) and with controllable circuits (15) for shunting its elementary counters (12) addressing the stages (31) of intermediate switches, and a handler (20, 21, 22) running a sequence of commands for reconfiguring the counter in the course of the accomplishment of its counting cycle.